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REVIEW ARTICLE

A Review of Data-Driven Methods for Fault Localization and Diagnosis in DFT-Enabled Circuit

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Abstract*— Design-for-Test (DfT) in scalable and efficient Network-on-Chip (NoC) architectures remains a significant concern of modern VLSI and System-on-Chip (SoC) design, which is the main source of stability, effectiveness, and error tolerance in complicated operational systems the widespread integration of multi-core processors and heterogeneous IP cores, NoCs have been the core of on-chip communication, thus the presence of robust testing strategies is essential On the one hand, techniques such as scan-based testing, Automatic Test Pattern Generation (ATPG), and Built-In Self-Test (BIST) are the pillars of fault detection and diagnosis, which identify permanently as well as transiently located faults in data modern Test Access Mechanisms (TAMs) and hierarchical testing frameworks that challenge the large-scale designs provide better observability and controllability an environment for the deployment of machine learning-assisted fault localization, which, due to their adaptive, scalable, and efficient nature, can handle the ever-increasing design complexity. An intelligent and data-driven approach to traditional DfT methods helps to accomplish more fault coverage, less test cost, and higher reliability.

***Keywords*– Design-for-Test (DfT), Network-on-Chip (NoC), Fault Models, fault identification and localization, System-on-Chip (SoC)**

I. INTRODUCTION

Fault diagnosis is a broad concept that encompasses multiple processes, including fault detection, isolation, identification, and reconstruction[1] [2]. Fault detection is the first step, focusing on determining whether a fault has occurred, while anomaly detection seeks to identify unusual patterns in system behavior before they evolve into critical failures [3][4]. Fault identification further categorizes the nature of the fault whether mechanical, electrical, or parametric while fault reconstruction estimates the magnitude of the fault using redundancy-based models[5][6]. Together, these processes form the foundation of Fault Detection and Diagnosis (FDD), which plays a vital role in ensuring system reliability and robustness across engineering applications.

a hardware product, “design for testability” conversely “design for test” acronymic as DFT comprises Integrated circuit (IC) design proficiencies that includes analysis characteristics. the distribution of passing and failing tests to infer likely fault on integrating Design-for-Testability (DFT) techniques with data-driven approaches to enhance fault localization and diagnosis. DFT mechanisms, such as scan chains, Built-in Self-Test (BIST), and boundary scan, improve the controllability and observability of circuits, thereby generating rich diagnostic data[7] Such deviations may include actuator blockages, sensor malfunctions, or component disconnections, all of which can alter the input output properties of the circuit and degrade system performance[8][9]. domains such as HVAC, transportation, and industrial automation, faults may not only cause inefficiencies but also pose risks to user safety and increase maintenance costs[10][11]. Similarly, in VLSI and System-on-Chip (SoC) designs, undetected faults can compromise circuit functionality, reduce yield, and demand costly redesigns. To address these challenges, the Fault Detection and Diagnosis (FDD) process aims to detect, locate, and analyze faults.

fault localization has emerged as a central area of study. Traditional approaches such as coverage-based fault localization assign suspiciousness scores to circuit or program elements based on test coverage data[12]. Techniques like Spectrum-Based Fault Localization (SBFL) utilize. Data-driven methods including machine learning, deep learning, and probabilistic models leverage this data to identify fault patterns, localize fault sites, By combining the structural[13][14]. DFT with the adaptive intelligence of data-driven techniques, modern fault diagnosis frameworks offer a more scalable, interpretable, and efficient solution for ensuring the reliability of VLSI and SoC designs.

1.1 Structure of the paper

The paper is organized as follows: Section II discusses Design-for-Testability (DFT) in modern circuits. Section III examines data-driven approaches for fault localization. Section IV extends the discussion to data-driven fault diagnosis. Section V reviews recent literature contributions and summarizes comparative studies. Finally, Section VI presents the conclusion and outlines future research directions

II. DESIGN-FOR-TESTABILITY IN MODERN CIRCUITS

Design-for-Testability (DFT) is an essential design methodology in modern integrated circuits that allows efficient detection, localization, and diagnosis of faults. As circuit complexity continues to increase, traditional testing methods often fail to provide sufficient fault coverage or require excessive time and cost[15]. DFT addresses these challenges by adding extra test logic and access paths within the circuit, which improve controllability and observability of internal nodes. Common techniques include scan-based testing, Built-in Self-Test (BIST), boundary scan mechanisms, and memory test and repair structures. These methods make it possible to detect both permanent and transient faults more effectively while reducing the dependency on external test equipment. In advanced technologies, DFT plays a critical role in improving chip reliability, reducing manufacturing test cost, and ensuring faster fault diagnosis, which ultimately supports higher yield and more robust circuit performance.

A. Principles of DFT in VLSI and SoCs

Design-for-Testability (DFT) in VLSI and SoCs integrates specialized design techniques to enhance circuit observability and controllability. It enables efficient fault detection, reduces testing complexity, and ensures reliable post-manufacturing validation.

1. **Enhanced Controllability and Observability** – DFT introduces additional test structures that improve access to internal circuit nodes[16], enabling effective application of test patterns and observation of circuit responses.
2. **Integration of Built-in Test Features** – Techniques such as scan chains, Built-in Self-Test (BIST), and memory testing modules are embedded to ensure automatic and efficient fault detection with minimal reliance on external testers.
3. **Fault Coverage and Diagnosis Accuracy** – DFT ensures higher fault coverage by systematically targeting stuck-at, transition, delay, and transient faults, thereby improving the accuracy of fault localization and diagnosis.
4. **Test Cost and Time Optimization** – By reducing dependency on complex external testing equipment and minimizing test cycles, DFT lowers manufacturing costs and accelerates the overall testing process in VLSI and SoCs.
5. **Reliability and Scalability** – DFT supports the reliability of increasingly complex SoCs by enabling scalable testing strategies that can handle diverse modules, IP cores, and interconnects in heterogeneous architectures.

B. Fault Models in Digital Circuits

Fault models serve as abstractions that represent physical defects within digital circuits, enabling systematic generation of test patterns and fault diagnosis strategies. The most widely used model is the stuck-at fault, where a signal line is assumed to be permanently fixed at logic ‘0’ or ‘1’, simplifying fault detection and ATPG implementation. Transition and delay fault models extend this concept to timing-related defects, capturing issues such as slow-to-rise or slow-to-fall signals that impact circuit performance at higher clock frequencies. Bridging faults occur when unintended connections form between two or more signal lines, often leading to short circuits or logic errors[17]. Open faults, such as broken interconnects or transistor-level disconnections, are especially critical in advanced technologies and require current-based or IDDQ testing for reliable detection. More recently, models for transient and intermittent faults have gained importance, as circuits in nanometer regimes are increasingly vulnerable to environmental variations, aging effects, and soft errors induced by radiation. By providing a simplified yet practical view of defects, fault models form the foundation of both traditional and data-driven test methodologies, ensuring effective fault localization and diagnosis in VLSI and SoCs

C. Traditional Test and Diagnosis Strategies

Traditional test and diagnosis strategies in digital circuits were primarily developed to detect structural faults and ensure functional correctness with minimal hardware overhead. These approaches rely on predefined fault models and systematic application of test patterns to evaluate circuit behavior. Functional testing verifies whether the circuit performs according to its intended specification, while structural testing focuses on identifying specific defect types such as stuck-at, transition, or bridging faults[18]. Automatic Test Pattern Generation (ATPG) plays a crucial role in producing effective test vectors that maximize fault coverage, and scan-based testing improves observability and controllability by transforming sequential circuits into easily testable structures. Diagnosis methods, such as fault dictionaries and simulation-based comparisons, are used to isolate fault locations once an error is detected. Although effective for permanent and manufacturing-related faults, these traditional strategies face limitations in handling intermittent, transient, and aging-induced defects, which are increasingly common in deep sub-micron VLSI and SoC designs.

III. DATA-DRIVEN APPROACHES FOR FAULT LOCALIZATION

Data-driven approaches for fault localization leverage statistical learning, machine learning, and deep learning techniques to analyze test responses and identify faulty regions within a circuit. Unlike traditional rule-based methods that rely solely on predefined fault models, data-driven strategies exploit large volumes of simulation and measurement data to uncover hidden patterns that correlate with fault behavior[19]. Supervised learning methods, such as support vector machines, decision trees, and random forests, have been widely applied to classify fault signatures and map them to potential fault sites. More recently, deep neural networks and convolutional architectures have been utilized to capture nonlinear dependencies between input–output patterns and fault locations with higher precision. Feature extraction from current, voltage, and delay measurements often enhanced by signal processing methods like Fourier or wavelet transforms further improves

fault localization accuracy. By continuously learning from new fault scenarios, these approaches not only enhance diagnostic resolution but also reduce the reliance on exhaustive test patterns, making them well-suited for complex and large-scale VLSI and SoC designs.

A. Machine Learning-Based Fault Identification

machine learning technique for link fault identification and localization [20]. it is imperative to identify the features to be extracted from network traffic measurements for localizing link disconnections in the network link reconnection and may correct the disconnected link resulted by the first stage in figure 1. Below, describe the details of each stage.

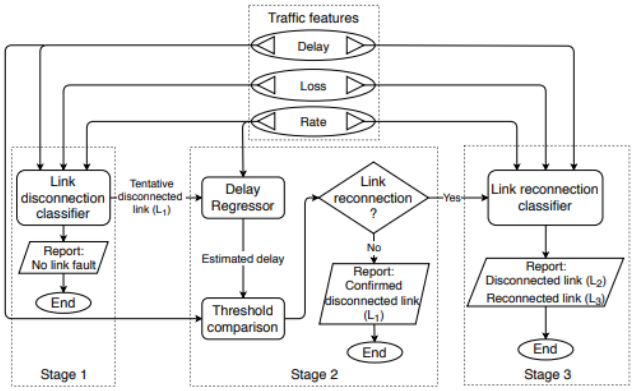

Figure 1. Block diagram of Machine learning fault identification and localization

1) *Link Disconnection Classification:* different link disconnections may cause different traffic behaviors represented by the traffic measurements the problem can be considered as a multi-class machine learning classification problem. where E is the set of links in the network[21]. Thus, the total the number of classes required for training the machine learning algorithm to detect and localize a link fault in the network. three traffic features and train the learning model using one of the following machine learning algorithms.

- Support Vector Machine (SVM) is a supervised machine learning technique that tries to separate data points into two different classes by identifying the best possible separating hyperplane.
- Random Forest (RF) is a classifier algorithm that constructs multiple decision trees during the training phase and outputs the mode of the individual trees as the class label.

machine learning algorithms that can be used for a classification problem, SVM, RF have demonstrated their best performance over other algorithms.

2) *Link* Fault Identification: To identify the link fault, we estimate the end-to-end delay of the network traffic caused by the disconnection of the tentative link L1, using aggregate flow rates captured from the network. The estimated end-to-end delay is compared with the actual delay captured from the network.
3) *Link Reconnection Classification:* that a link reconnection has been identified by the second stage, the third stage of ML-LFIL localizes both disconnected link (L2) and reconnected link (L3) using a link reconnection classifier. The disconnected link L2 might be different or the same as the tentative disconnected link L1 depending on the accuracy of the link disconnection classifier. Similar to link disconnection classification, link reconnection classification in the third stage of ML-LFIL (ML-LFIL-S3) is also a multiclass machine learning classification problem.

B. Deep Learning Architectures for Fault Mapping

The categorization of major DL-based approaches used in intelligent FDP. According to the supervision type, they can be divided into unsupervised methods and supervised methods. The former tries to find the inherent common pattern within data which are unlabeled, while the latter refers to methods that learn highly non-linear relationship between the input data and its paired labeled output[22]. More specifically, the supervised methods can be further divided into processing of specific data types or extraction of distinctive features, depending on their objectives. Their detailed expanded in the following sections in figure 2.

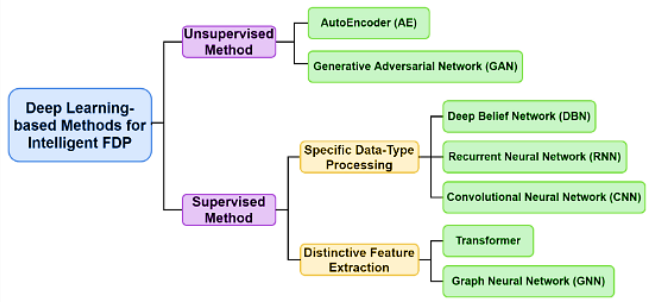

Figure 2. The categorization of deep learning techniques in intelligent FDP

the categorization of major DL-based approaches used in intelligent FDP. According to the supervision type, they can be divided into unsupervised methods and supervised methods. The former tries to find the inherent common pattern within data which are unlabeled, while the latter refers to methods that learn highly non-linear relationship between the input data and its paired labeled output DL architectures include deep belief network (DBN), autoencoder (AE), convolutional neural network (CNN) , and RNN . With the rapid development of DL techniques in these years, many new architectures have been proposed and introduced into the tasks of intelligent industrial FDP. Examples are generative adversarial network (GAN), transformer, and graph neural network (GNN).

C. Statistical and Probabilistic Inference Methods

Four probabilistic models applied in the field of FDD are illustrated, including probabilistic PCA, probabilistic PLS, probabilistic ICA, probabilistic canonical correlation analysis (CCA), and probabilistic Fisher discriminant analysis (FDA). PCA extracts the principal components that are retained to explain the majority of the variability in the data by maximizing

the variance. Compared to PCA, the FDA maximizes the separation among classes while minimizing the separation between classes[23]. The components after PCA decomposition are orthogonal and therefore irrelevant, but independence is not guaranteed. Compared to PCA, ICA can find the original components in the observed mixtures, and it is a linear transformation of the data in the original feature space. PCA involves only one set of variables, while CCA extends to the interdependence between two sets of variables, measuring the correlation between the two sets of variables.

IV. DATA-DRIVEN APPROACHES FOR FAULT DIAGNOSIS

Data-driven approaches present challenges due to the complexity of specific systems, where traditional methods may be impractical due to limitations in modeling or available expertise. Data-driven techniques leverage AI and Machine Learning to extract insights directly from data, complementing traditional methods with adaptability and scalability[24]. This evolution highlights the transformative role of AI and ML in Fault Detection and Diagnosis, as detailed in the following section. AI involves creating systems that possess human-like cognitive functions such as learning, reasoning, and problem-solving. Its application ranges widely from autonomous vehicles to healthcare diagnostics. On the other hand, ML is a crucial subset of AI that enables machines to learn from data, thereby revolutionizing the way complex problems are tackled. It includes techniques like logistic regression and Neural Networks, which are essential in various industries, including fault detection and process optimization

A. Classification of Fault Diagnosis Methods

There is great quantity of literature on dynamic systems fault diagnosis ranging from analytical methods to artificial intelligence and statistical approaches. From a modelling prospective, there are methods that require accurate system models (plants), quantitative models or qualitative models. However, there are methods that do not require any form of model information and rely only on historic system data. Classification of fault diagnosis methods is presented in this paper based on the contributions of various researchers. This classification of fault diagnosis methods is shown in Figure 3. Fault diagnosis methods are broadly classified into three main categories: model-based, hardware-based and history-based

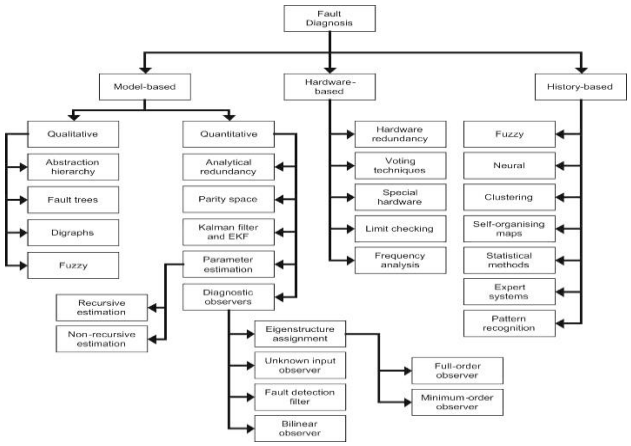

Figure 3. Classification of fault diagnosis methods

While there have been some excellent reviews in the field of fault diagnosis, it is of interest that classification of fault diagnosis methods very often is not consistent. This is mainly due to the fact that researchers are often focused on a particular branch, such as analytical models, of the broad discipline of fault diagnosis.

B. Bayesian and Graph-Based Models

Fault diagnosis scheme based on Bayesian network proposed in this paper is designed to localize faulty system components that cause the abnormal behaviors of a system or process, rather than generating an initial fault candidates' set[25]. A probability distribution, which is computed through the Bayesian network with given evidence, is attached to each system component. Hence, ranking of faulty system components can be achieved. Faulty system components to be localized are represented as hypothesis variables in the network and system measurements are input to the network through the corresponding information variable. This has a close relation with bond graph model. Components in bond graph are represented as C, I, or R, elements, while system measurements are represented as corresponding effort or flow in the bond graph.

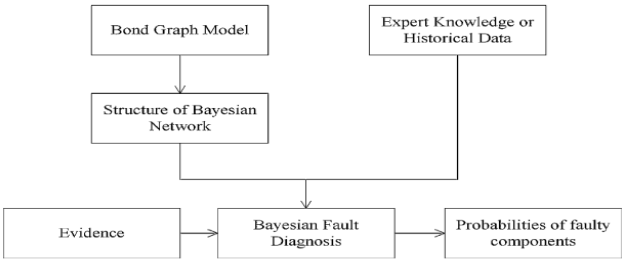

Figure 4. the proposed fault diagnosis based on Bayesian network

Figure 4 illustrates the fault diagnosis scheme based on Bayesian network. A bond graph model from a system concerned is used to construct a Bayesian network for localizing faulty system components. Once the structure of the diagnostic Bayesian network is known and the necessary CPDs are acquired from either historical data or expert knowledge, the Bayesian fault diagnosis module is activated. System

measurements are provided to the Bayesian fault diagnosis module as evidences input to the network.

C. Hybrid Fault Diagnosis Approach

Model-based, signal-based, and knowledge-based fault diagnosis methods have their distinctive advantages and various constraints. Specifically, model-based fault diagnosis can monitor and diagnose unknown faults by using a small amount of real-time data, but it requires an explicit model representing the input–output relationship; the diagnosis performance relies on the model accuracy[26]. On the other hand, signal-based and knowledge-based approaches do not require an explicit or complete model, which are particularly suitable for monitoring and diagnosis for complex industrial processes where explicit system models are unavailable or challenging to derive. The signal-based method generally extracts the major features of the output signals for fault diagnosis, but it pays less attention on system dynamic inputs, whose diagnosis performance may be thus degraded under unknown input disturbances or unbalanced conditions. Due to the high dependence on a large amount of historical data for training, the knowledge-based method suffers high computational costs and may not work well for identifying unknown fault types.

D. Challenges in data driven fault Localization and diagnosis

Data-driven fault localization and diagnosis in modern circuits are hinder by numerous technical and practical limitations that arise from the growing complexity and variability of the design. These issues have an impact on the performance, scalability, and trustworthiness of machine learning–based diagnostic methods when used in various technologies. The main challenges are outlined below and clarified:

1. Limited Availability of labeled fault data

Data-driven models, notably deep learning architectures, need a massive amount of precisely labeled faulty data to be trained. But in the case of real semiconductor setups, it is quite challenging to come up with such datasets[27]. Artificial data can be created through fault injection, yet it is usually incapable of representing the complexity and variability of the actual silicon defects.

2. Data imbalance and noise in test response

Most of the devices are without faults, and defective samples make up only a very small part of the dataset[28]. Such an imbalance makes machine learning models biased toward predicting fault-free behavior and thus less sensitive to rare but important failures. Additionally, test responses can include noise due to environmental changes, measurement inaccuracies, and intermittent behavior.

3. Data Availability and Quality

Accurate ML models are only possible if we have high-quality runtime telemetry data. Yet there are issues of privacy concerns, lack of standardization over the broad range of various SoC architecture designs, and noisy or missing telemetry data as obstacles to data collection. This poor quality of data can have negative effects on the model's performance.

4. Scalability Challenges for Large and Complex SoCs

Modern system-on-Chip (SoC) architectures entail a staggering number of transistors in the billions, various IP cores, and different functional blocks, which in turn makes fault diagnosis an intricate challenge of a very high degree[29]. The data-driven approaches have to handle very large test data sets, circuit graphs, and fail logs, all of which require a substantial amount of computational resources. Deep neural networks and graph-based learning techniques might find it difficult to scale efficiently with the growth of the circuit size.

5. Difficulty in modeling dynamic and transient fault

Transient faults, intermittent defects, and failures caused by aging are inherently non-pattern phenomena, hence it is quite a challenge to use fixed learning models to capture them. Such faults can happen at random intervals due to changes in the environment, cosmic radiation events, or the natural aging of the device conventional data-driven models that are trained on static datasets rarely have the capability to detect or anticipate these faults.

1. LITERATURE OF REVIEW

This literature Summary synthesizes recent advancements in data-driven fault localization and diagnosis within DFT-enabled circuits, emphasizing neural networks, hybrid analytical approaches, probabilistic models.

Wu *et al.*, (2025) a model-based fault detectability analysis method is proposed to establish the measurement conditions necessary for reliably detecting various fault types. Utilizing these measurement condition constraints, a mechanism-enhanced neural network is designed to locate faults by fitting the changes in fault parameters. The consistency between the fitting fault parameters and the actual fault process ensures the interpretability of the diagnosis results guaranteeing the identification of fault parameters, the fault circuit model assists in training, significantly reducing the number of actual fault samples required for mechanism-enhanced neural network training[30].

Jois and V, (2024) implementing DFT techniques to enhance testing efficiency and effectiveness. Key components like JTAG compliant Registers, IJTAG-controlled Segment Bits, Memory Built-in Self-Test, Memory repair modules, and Boundary Scan mechanisms are strategically integrated into the design. Automatic Test Pattern Generation (ATPG) and thorough simulations validate the effectiveness of these DFT strategies the importance of the requirement and design of the security feature for the IJTAG network to provide protection against unauthorized access of the network ensuring the improvement in robustness of the Integrated Circuit[31].

Lai *et al.*, (2024) a hybrid method for diagnosing single and multiple transistor open-circuit faults in grid-tied three-phase voltage source inverters. Combining explicit variable relationships in analytical models with the nonlinear regression capability of neural networks, the method comprises offline model training and online fault diagnosis sections. The offline section constructs a neural network model based on analytical

model variables, using closed-loop system samples to predict fault characteristics. In the online part, the predictive model is applied to the Simulink online simulation platform[32].

Hamatwi *et al.*, (2023) the performance of three high impedance fault detection techniques for the case of a distribution network to select the technique that is best suited for detecting faults in this network. discrete Fourier transform, discrete wavelet transforms, and the power spectrum among other techniques were selected. The distribution network was modelled in MATLAB/Simulink, along with the High Impedance Fault condition. These fault detection techniques were modelled and applied separately to the distribution network under different operating conditions high impedance fault, load switching, and normal operation[33].

Fang *et al.*, (2022) a data-driven scheme based on Random Vector Functional Link (RVFL) network with data dimension reduction capability is proposed to diagnose the power switch open-circuit faults of the multiphase inverter. The enhanced fast Fourier transform (FFT) considering the rotational speed of the motor is adopted to extract the phase current features precisely, and then the dimensions of data are reduced through the Relief algorithm. At last, the faults are detected and diagnosed by the RVFL network. Simulation experiments and comparison analysis are conducted on a six-phase permanent magnet synchronous motor (PMSM) drive system, which demonstrate that the proposed method can effectively extract fault features and achieve high accuracy while reducing the computational effort[34].

Jiang, (2021) a data-driven probabilistic fault location methodology based on comprehensive sensing measurement from digital relays at substations, Intelligent Electric Devices (IEDs) along primary feeders, SCADA sensors in the feeder circuit, and smart meters at customers' premises. Statistics of historical fault location accuracies by digital relays and IEDs are used to estimate fault location errors. Multiple-hypothesis analysis is implemented to handle the uncertainties from SCADA sensors and smart meters. The spatial correlation between the potential fault location and collected sensor data is modeled as a mixed integer linear programming (MILP) problem[35].

Table 1 presents a comparative summary of recent studies on data-driven fault localization and diagnosis in DFT-enabled circuits, highlighting applied approaches, key contributions, associated challenges, and prospective research directions.

Table 1 Summary of a Study on Data-Driven Methods for Fault Localization and Diagnosis in DFT-Enabled Circuit

Author	Study On	Approach	Key Findings	Challenges	Future Directions
Wu et al., (2025)	Fault detectability analysis with mechanism-enhanced neural networks	Model-based detectability constraints + NN for parameter fitting	Ensures interpretability and reduces training samples needed by integrating circuit models	Requires accurate modeling of measurement constraints; limited by complex fault interactions	Extend to large-scale SoCs and adaptive online training
Jois and V, (2024)	DFT strategies for improved testing	Integration of JTAG, IJTAG, MBIST, repair modules, boundary scan + ATPG	Enhances testing efficiency and robustness with security features in IJTAG	Overhead in integrating multiple modules; vulnerability to evolving security threats	Develop low-overhead, AI-assisted secure DFT frameworks
Lai et al., (2024)	Hybrid diagnosis of open-circuit transistor faults in inverters	Analytical models + neural networks (offline training, online simulation)	Accurate diagnosis of single and multiple transistor faults using combined offline-online strategy	Dependence on accurate modeling and simulation; computational cost	Real-time hardware implementation and adaptive learning models
Hamatwi et al., (2023)	High impedance fault detection in distribution networks	Comparative evaluation of DFT, DWT, and power spectrum methods in MATLAB/Simulink	Identified suitable techniques for detecting high impedance faults under varying conditions	Sensitivity to noise and operational variability	Develop hybrid multi-resolution detection methods with ML integration
Fang et al., (2022)	Fault diagnosis in multiphase inverters	FFT + Relief algorithm for feature extraction + RVFL neural network	High accuracy diagnosis with reduced computational cost	Dependence on precise feature extraction; limited generalization	Apply deep learning and transfer learning for broader applicability
Jiang, (2021)	Probabilistic fault location in power distribution	Data-driven MILP with multiple sensor inputs (IEDs,	Improved fault location accuracy by leveraging	High complexity of MILP; real-time	Scalable probabilistic frameworks for

		SCADA, smart meters)	probabilistic sensor data fusion	implementation issues	smart grids with adaptive data fusion

2. CONCLUSION AND FUTURE WORK

Design-for-Test (DfT) in scalable and high-performance Network-on-Chip (NoC) architectures is a critical aspect Testing is still a crucial issue in VLSI and SoC designs, which are the main sources of functionality, reliability, and long-term system sustainability. Various methodologies such as fault models, ATPG, scan-based testing, and BIST have been evolved over the years to provide structured approaches for fault detection and diagnosis. But the increasing complexity of the design makes traditional techniques less scalable, efficient, and capable of handling transient or intermittent faults. To overcome these problems, Design-for-Testability (DFT) principles have been implemented to large-scale systems, thus improving controllability, observability, and fault coverage. Moreover, the latest developments in data-driven methods, especially machine learning and probabilistic approaches, give the localization of faults a new direction in terms of accuracy and adaptability. The integration of classical DFT tactics with contemporary intelligent frameworks is a landmark transition toward comprehensive test solutions. However, there are still limitations in scaling to heterogeneous SoCs and guaranteeing real-time diagnosis. future should, among other things, concentrate on the integration of resourceful and adaptive fault detection models that are capable of working with advanced DFT architectures so as to take care of the issue of scalability in very complex SoCs. The point of the hybrid methods that merge the conventional strategies with the AI-driven ones should be the real-time diagnosis, the hardware overhead reduction, and the energy-efficient fault localization, i.e., in this way, the last-mentioned three problems will be resolved.

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